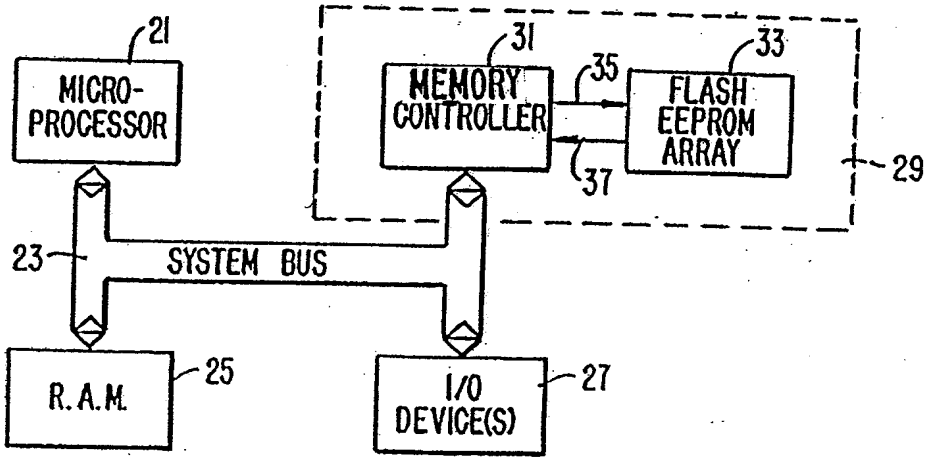

21
MICRO-PROCESSOR
31
MEMORY CONTROLLER
35
37
33
FLASH EEPROM ARRAY
29
23
SYSTEM BUS
R.A.M.
25
I/O DEVICE(S)
27

FIG._1A

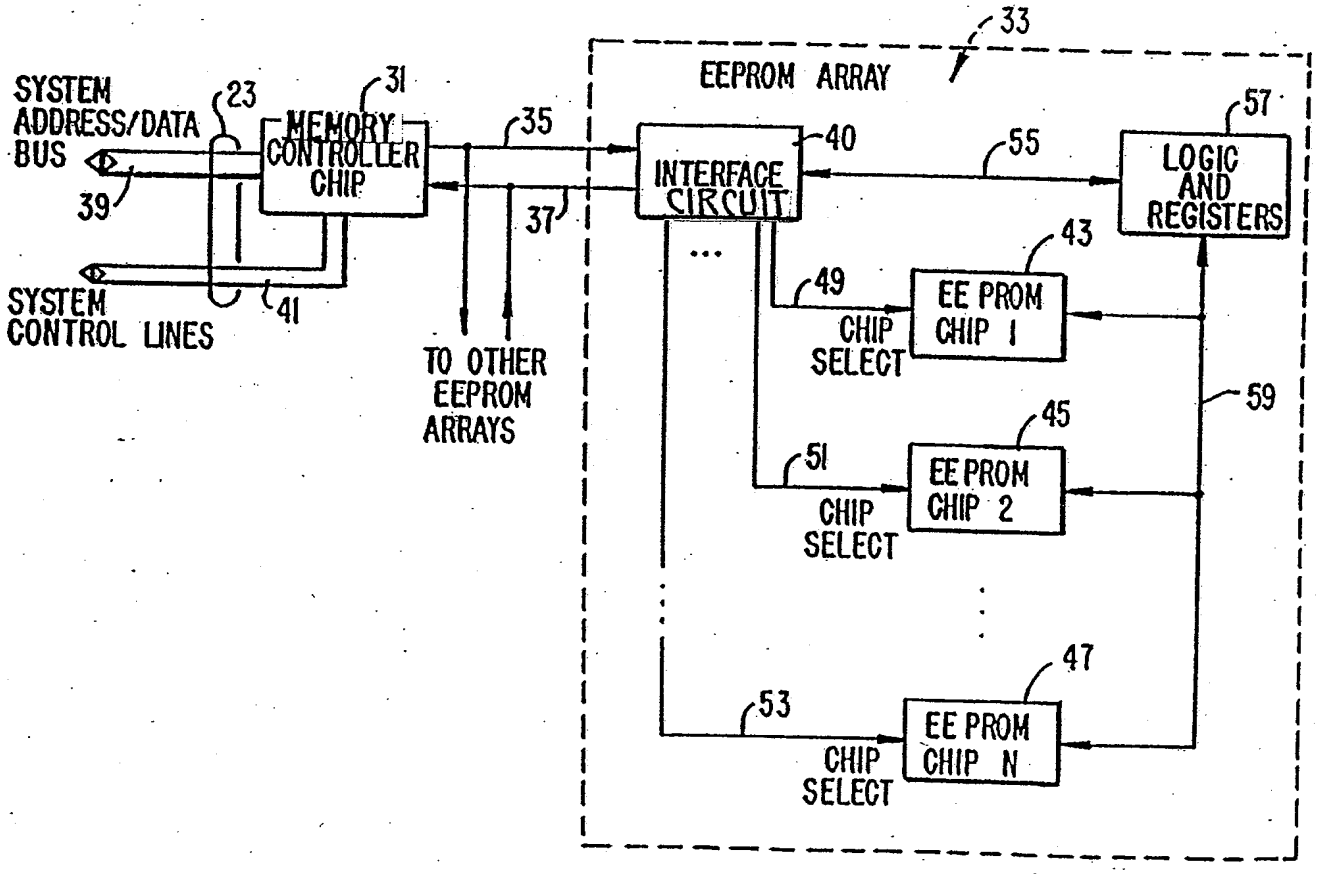

33
EEPROM ARRAY
SYSTEM ADDRESS/DATA BUS
23
31
MEMORY CONTROLLER CHIP
35
37
39
41
SYSTEM CONTROL LINES
TO OTHER EEPROM ARRAYS
INTERFACE CIRCUIT
40
55
57
LOGIC AND REGISTERS
43
49
CHIP SELECT
EE PROM CHIP 1
45
51
CHIP SELECT
EE PROM CHIP 2
59
47
53
CHIP SELECT
EE PROM CHIP N

FIG._1B

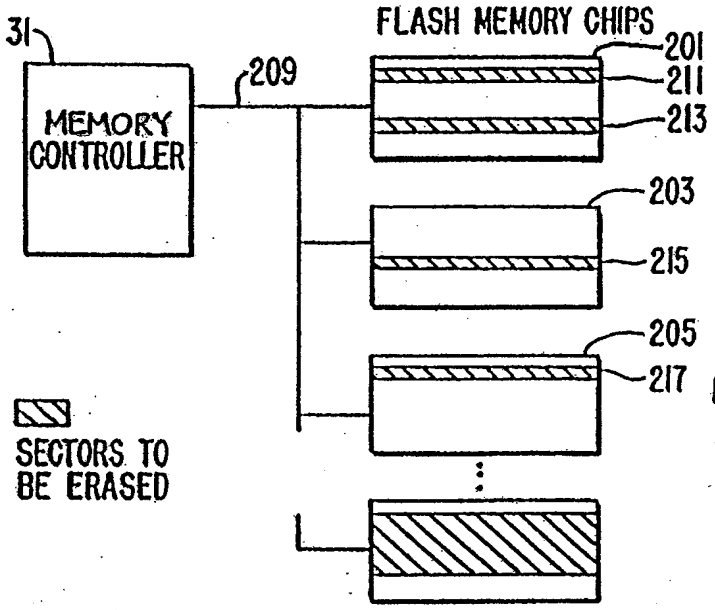


FIG._2

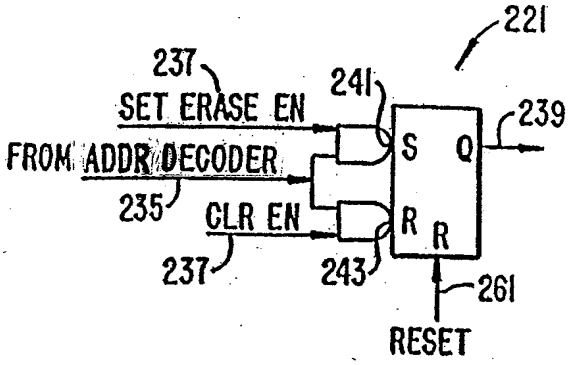


FIG._3B

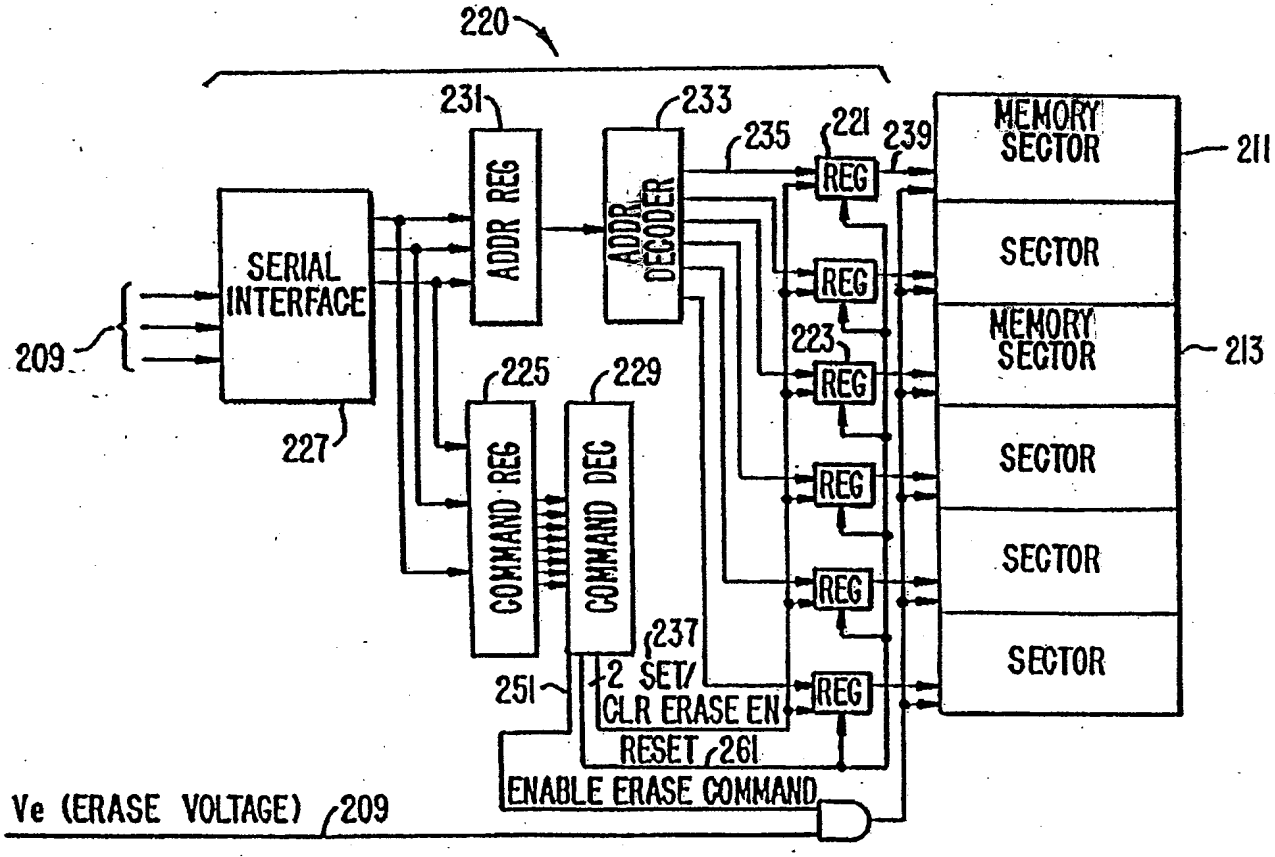
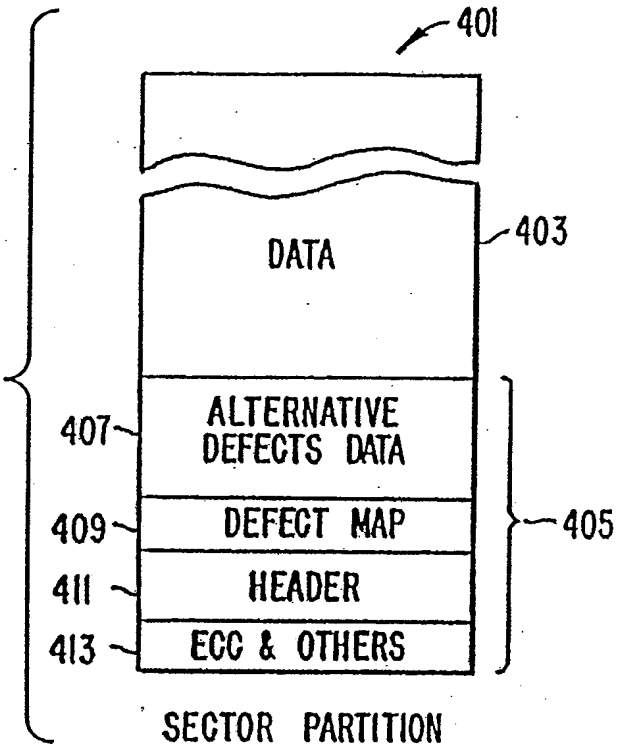


FIG._3A

FIG._5


401
DATA
403
ALTERNATIVE DEFECTS DATA
407
DEFECT MAP
409
HEADER
411
ECC & OTHERS
413
405
SECTOR PARTITION

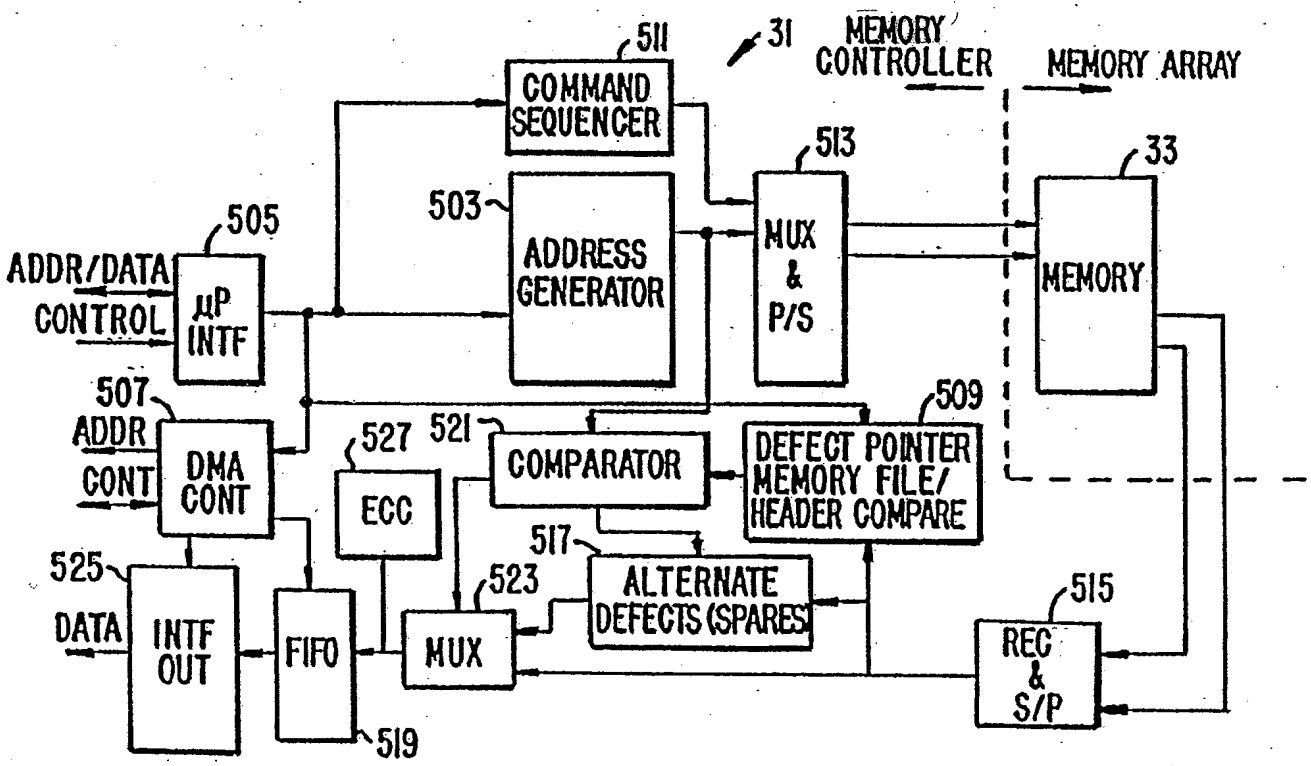

511
31
MEMORY CONTROLLER
MEMORY ARRAY
COMMAND SEQUENCER
513
33
503
505
ADDRESS GENERATOR
MUX & P/S
MEMORY
ADDR/DATA
CONTROL
μP INTF
507
509
ADDR
CONT
DMA CONT
527
521
COMPARATOR
DEFECT POINTER MEMORY FILE/ HEADER COMPARE
ECC
517
525
523
515
ALTERNATE DEFECTS (SPARES)
DATA
INTF OUT
FIFO
MUX
REC & S/P
519
READ DATA PATH CONTROL

FIG._6

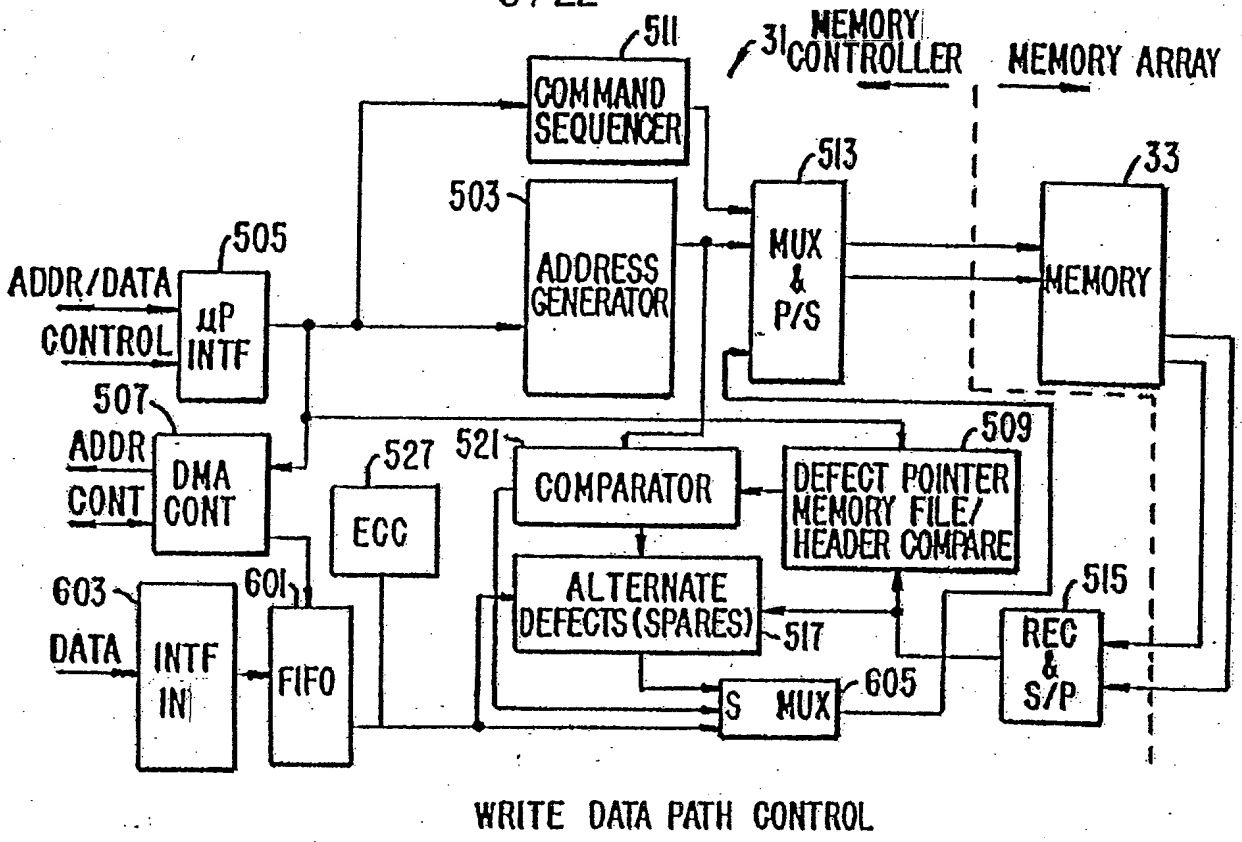

511
31
MEMORY CONTROLLER
MEMORY ARRAY
COMMAND SEQUENCER
513
33
503
ADDRESS GENERATOR
MUX & P/S
MEMORY
505
ADDR/DATA
CONTROL
μP INTF
507
ADDR
CONT
DMA CONT
527
ECC
521
COMPARATOR
509
DEFECT POINTER MEMORY FILE/ HEADER COMPARE
603
DATA
INTF IN
601
FIFO
ALTERNATE DEFECTS (SPARES)
517
515
REC & S/P
S MUX
605
WRITE DATA PATH CONTROL

FIG._7

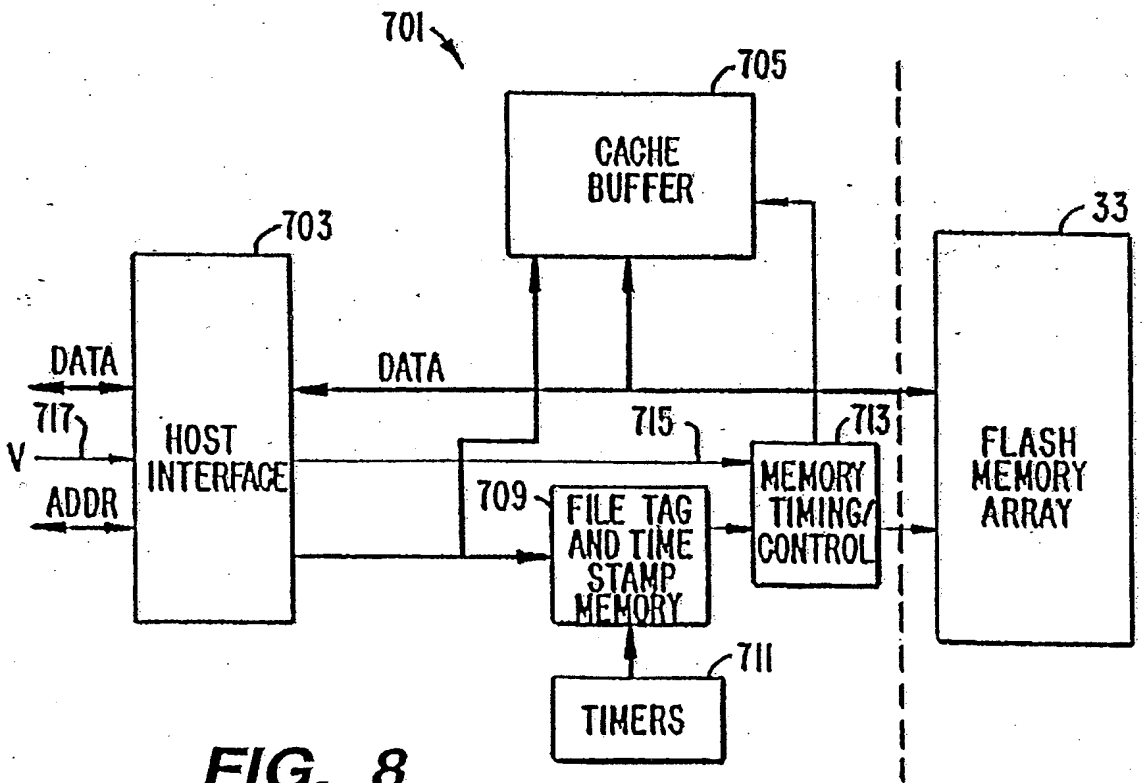

701
705
CACHE BUFFER
703
33
DATA
DATA
717
V
ADDR
HOST INTERFACE
715
713
709
FILE TAG AND TIME STAMP MEMORY
MEMORY TIMING/ CONTROL
FLASH MEMORY ARRAY
711
TIMERS

FIG._8

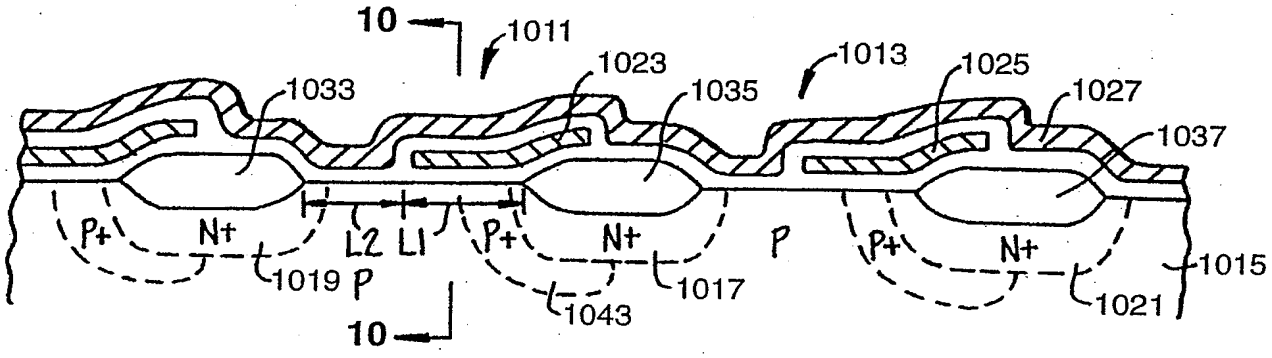


FIG._9

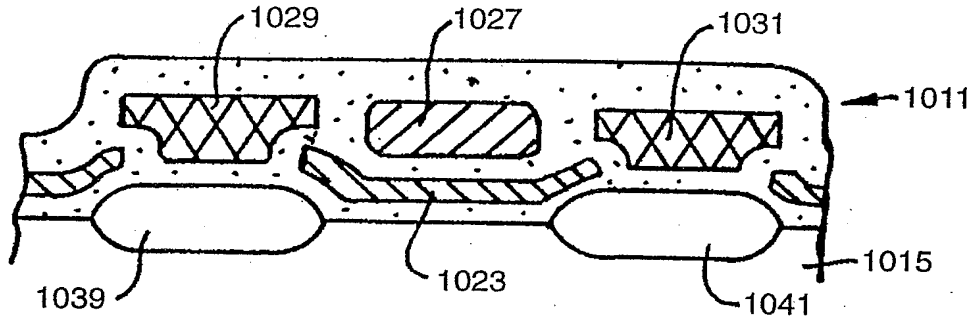


FIG._10

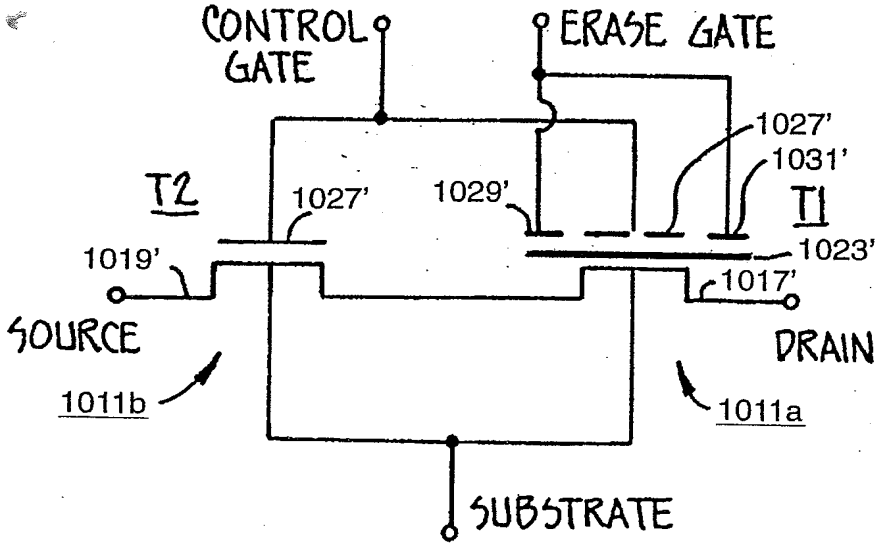


FIG._11

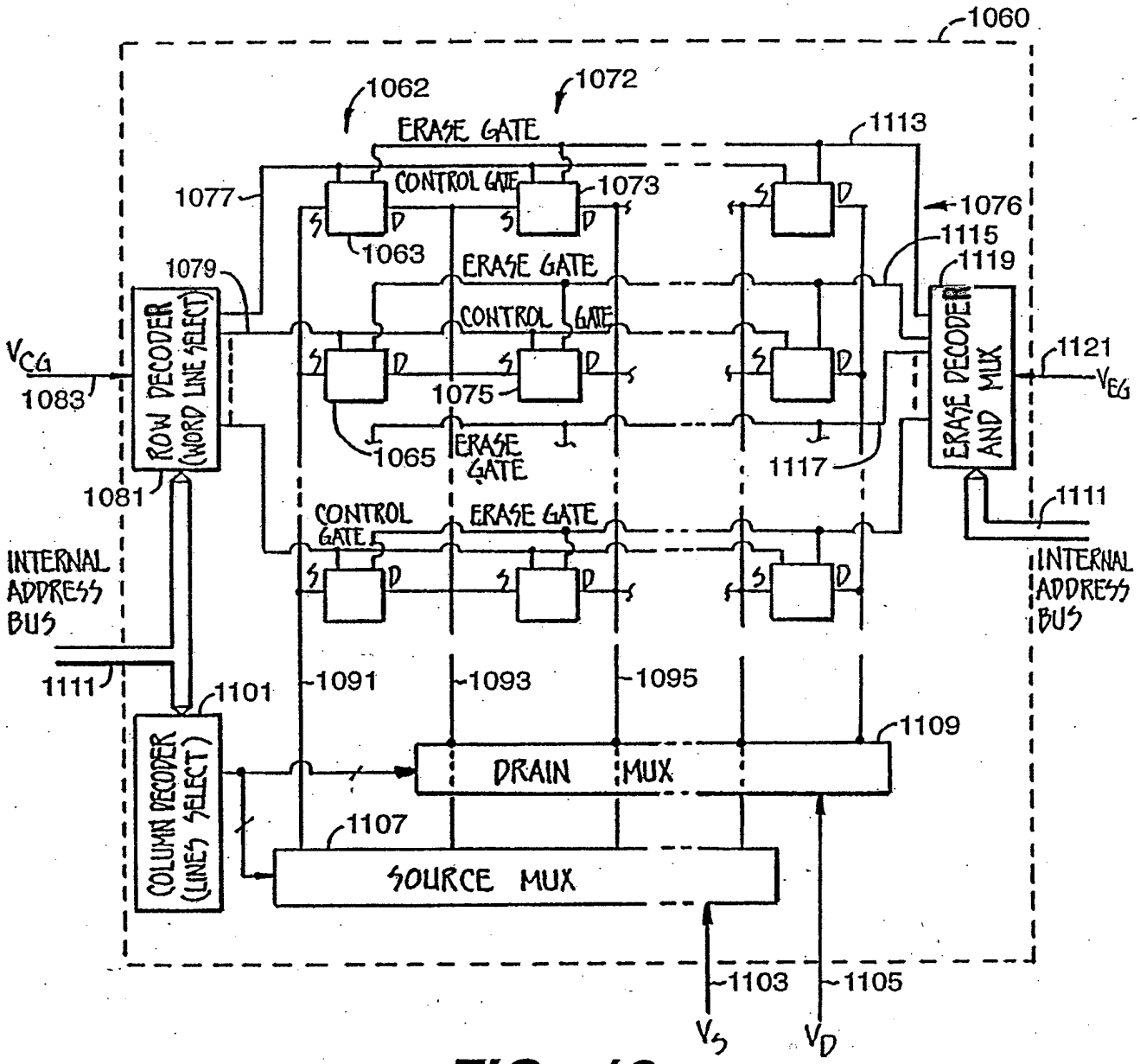

1060
1062
1072
ERASE GATE
1113
CONTROL GATE
1073
1077
1076
1063
1115
1119
ERASE GATE
1079
CONTROL GATE
ROW DECODER (WORD LINE SELECT)
ERASE DECODER AND MUX
V_{CG}
1083
1075
1121
V_{EG}
1065
ERASE GATE
1117
1081
CONTROL GATE
ERASE GATE
1111
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
1111
1101
1091
1093
1095
1109
COLUMN DECODER (LINES SELECT)
DRAIN MUX
1107
SOURCE MUX
1103
1105
V_S
V_D

FIG._12

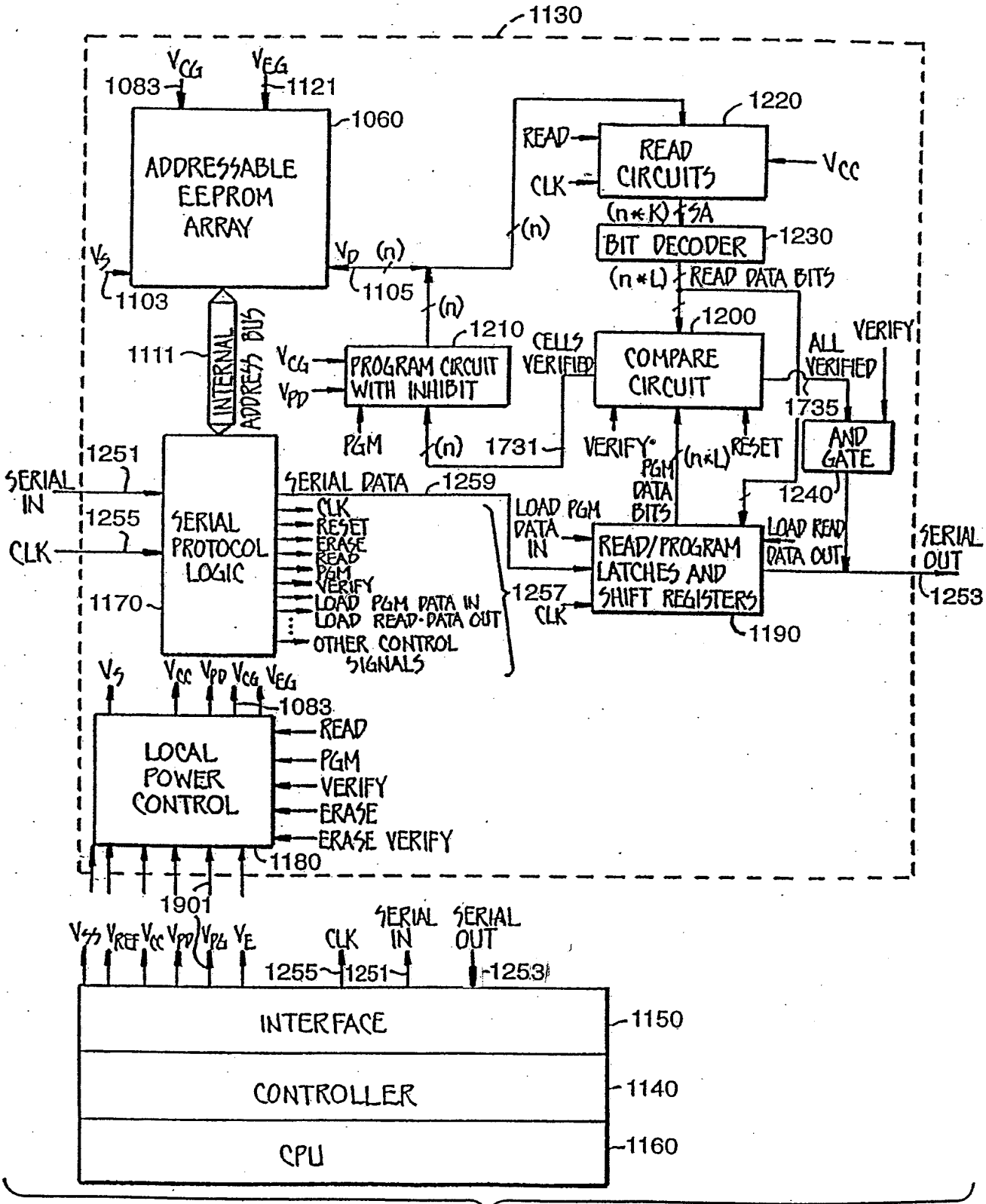

1130
ADDRESSABLE EEPROM ARRAY
1060
1083
1121
1103
1105
INTERNAL ADDRESS BUS
1111
READ CIRCUITS
1220
READ
CLK
BIT DECODER
1230
READ DATA BITS
PROGRAM CIRCUIT WITH INHIBIT
1210
COMPARE CIRCUIT
1200
CELLS VERIFIED
ALL VERIFIED
VERIFY
1735
AND GATE
1240
PGM
1731
VERIFY*
RESET
SERIAL IN
1251
SERIAL PROTOCOL LOGIC
1255
CLK
1170
SERIAL DATA
1259
CLK
RESET
ERASE
READ
PGM
VERIFY
LOAD PGM DATA IN
LOAD READ-DATA OUT
OTHER CONTROL SIGNALS
LOAD PGM DATA IN
PGM DATA BITS
READ/PROGRAM LATCHES AND SHIFT REGISTERS
1257
1190
LOAD READ DATA OUT
SERIAL OUT
1253
LOCAL POWER CONTROL
READ
PGM
VERIFY
ERASE
ERASE VERIFY
1180
1901
INTERFACE
1150
CONTROLLER
1140
CPU
1160

FIG._13

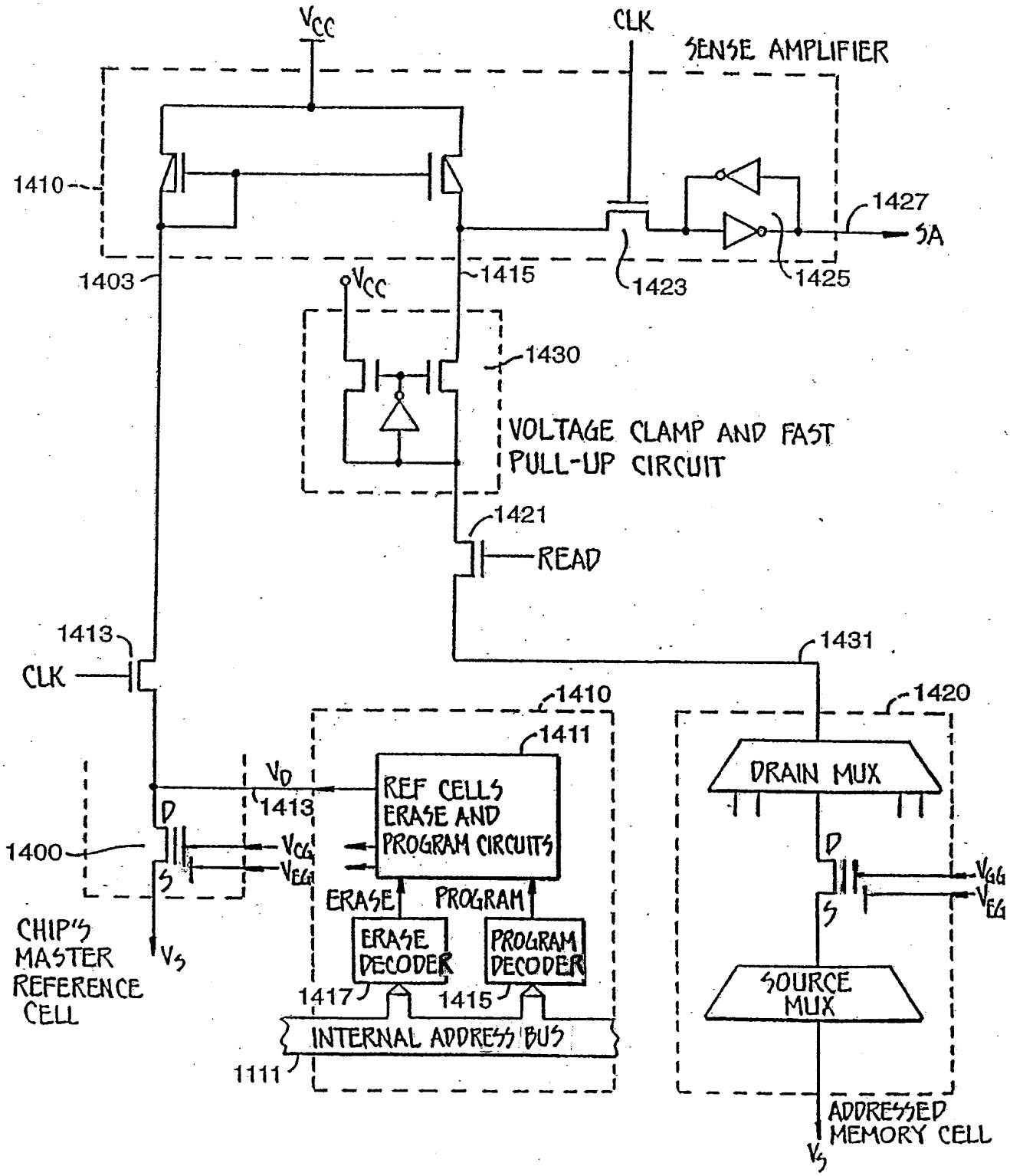

V_{CC}
CLK
SENSE AMPLIFIER
1410
1427
SA
1403
1415
1423
1425
V_{CC}
1430
VOLTAGE CLAMP AND FAST PULL-UP CIRCUIT
1421
READ
1413
CLK
1431
1410
1420
1411
V_D
1413
REF CELLS ERASE AND PROGRAM CIRCUITS
DRAIN MUX
D
1400
V_{GG}
V_{EG}
S
ERASE
PROGRAM
CHIP'S MASTER REFERENCE CELL
V_S
ERASE DECODER
PROGRAM DECODER
SOURCE MUX
1417
1415
INTERNAL ADDRESS BUS
1111
ADDRESSED MEMORY CELL
V_S

FIG._17A

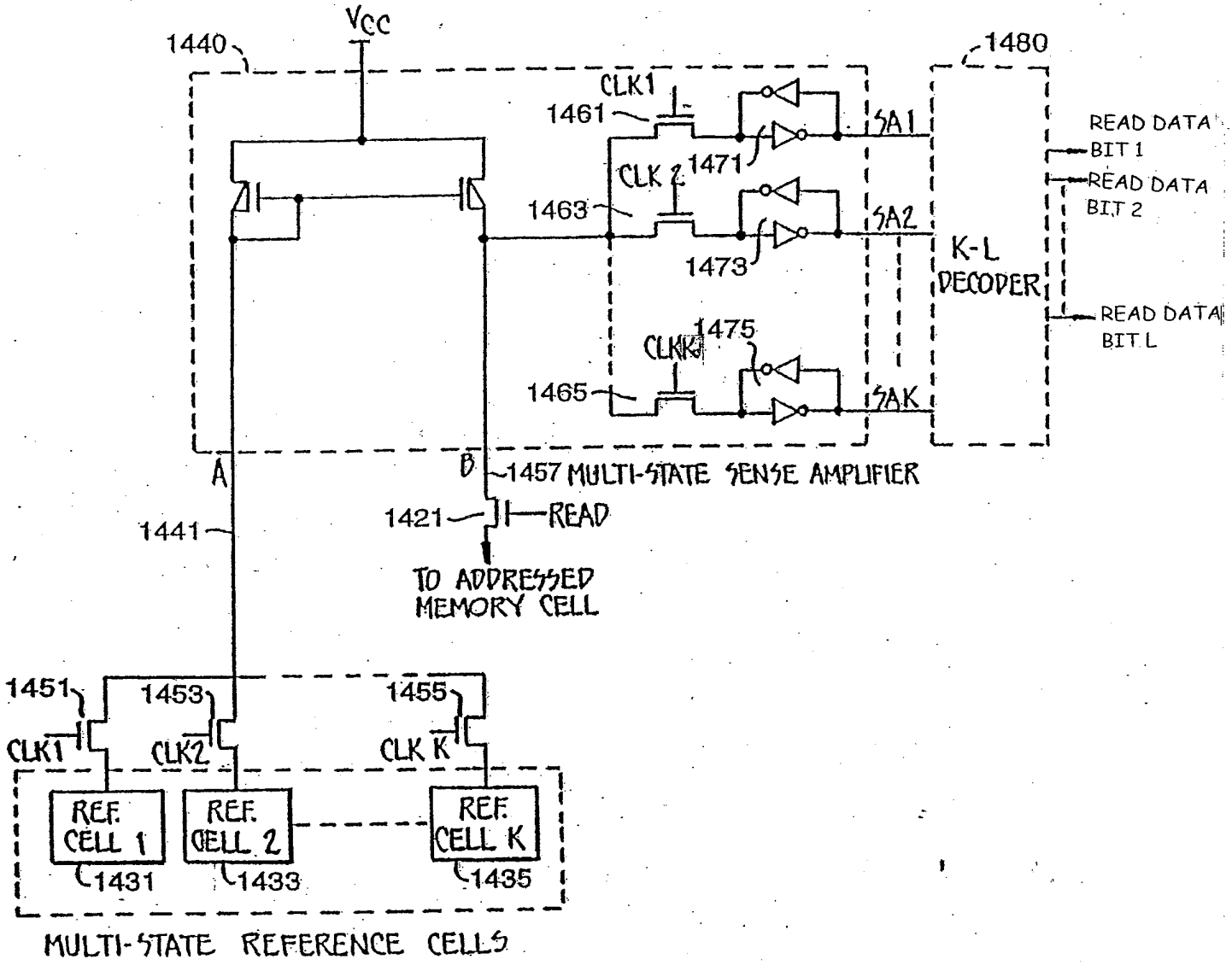

Vcc
1440
1480
CLK1
1461
1471
SA1
READ DATA BIT 1
CLK 2
1463
SA2
READ DATA BIT 2
1473
K-L DECODER
1475
CLKK
1465
SAK
READ DATA BIT L
A
B
1457 MULTI-STATE SENSE AMPLIFIER
1421
READ
1441
TO ADDRESSED MEMORY CELL
1451
1453
1455
CLK1
CLK2
CLK K
REF. CELL 1
REF. CELL 2
REF. CELL K
1431
1433
1435
MULTI-STATE REFERENCE CELLS

FIG._17B

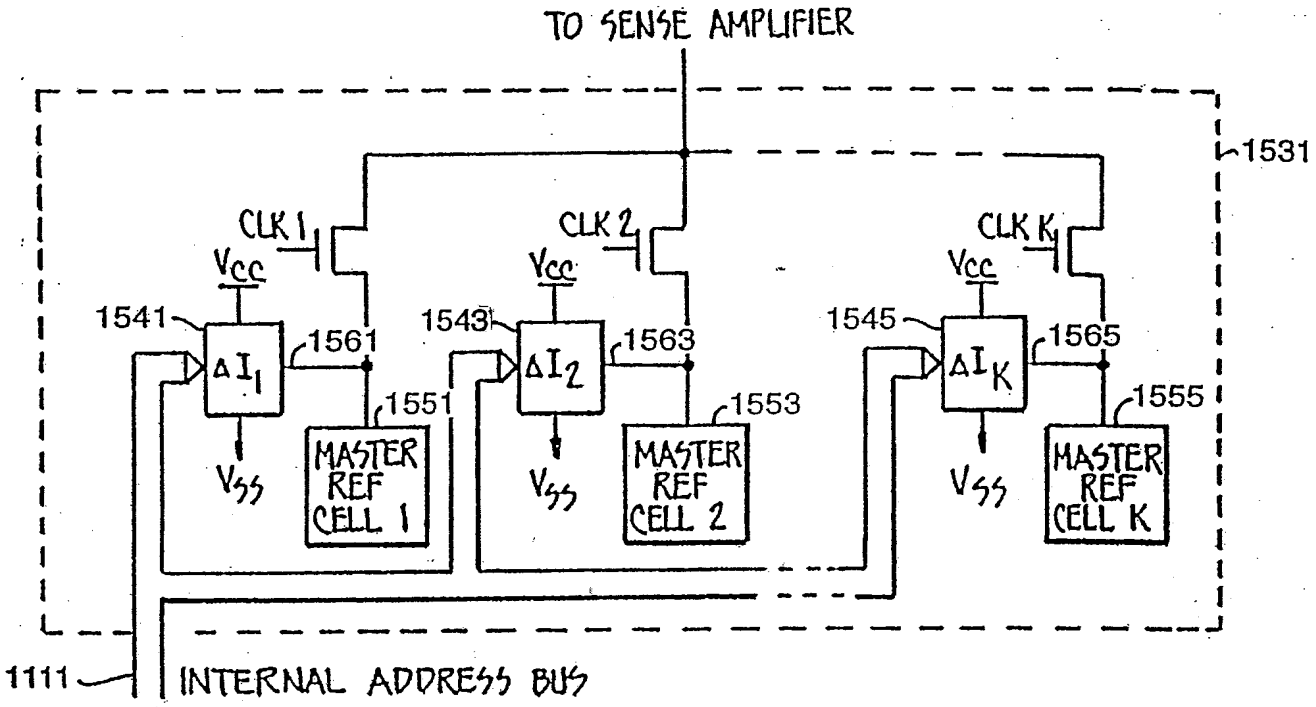


FIG._21B

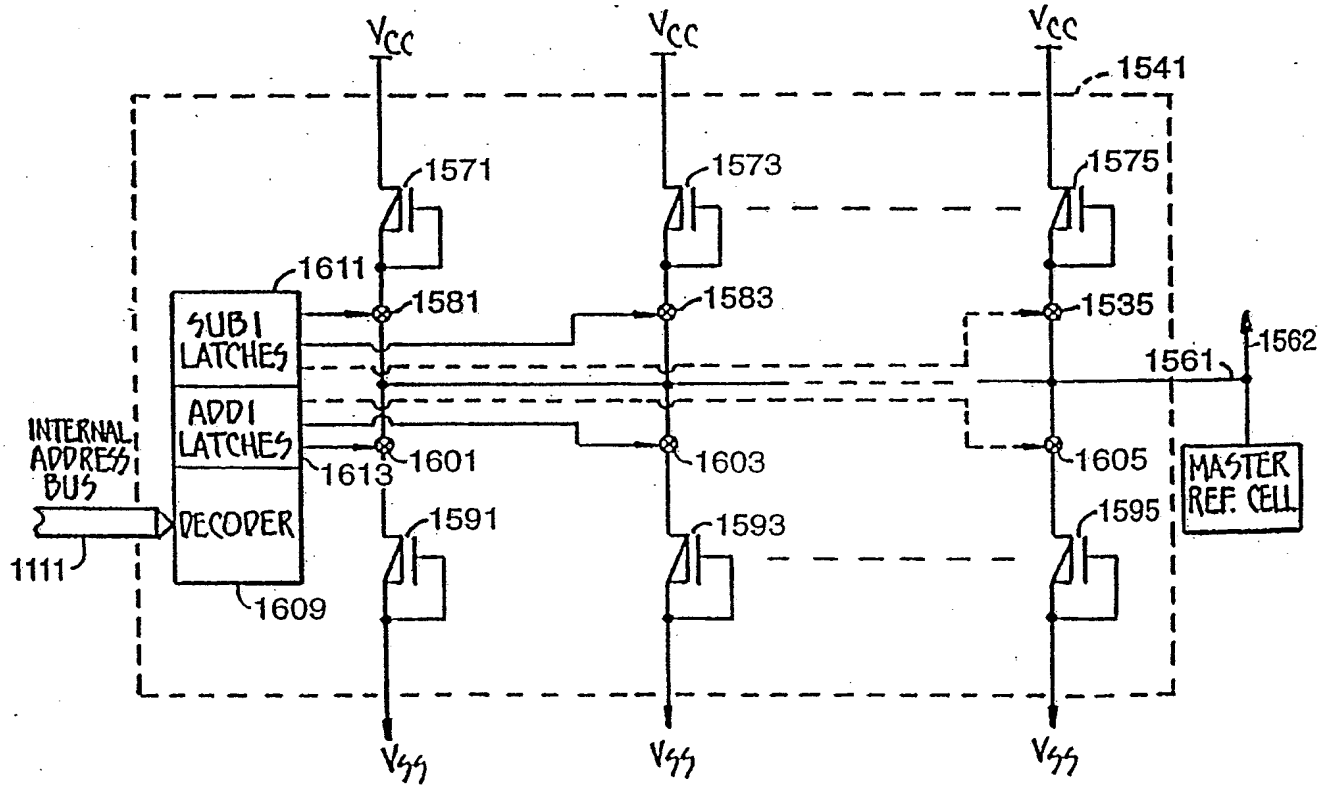
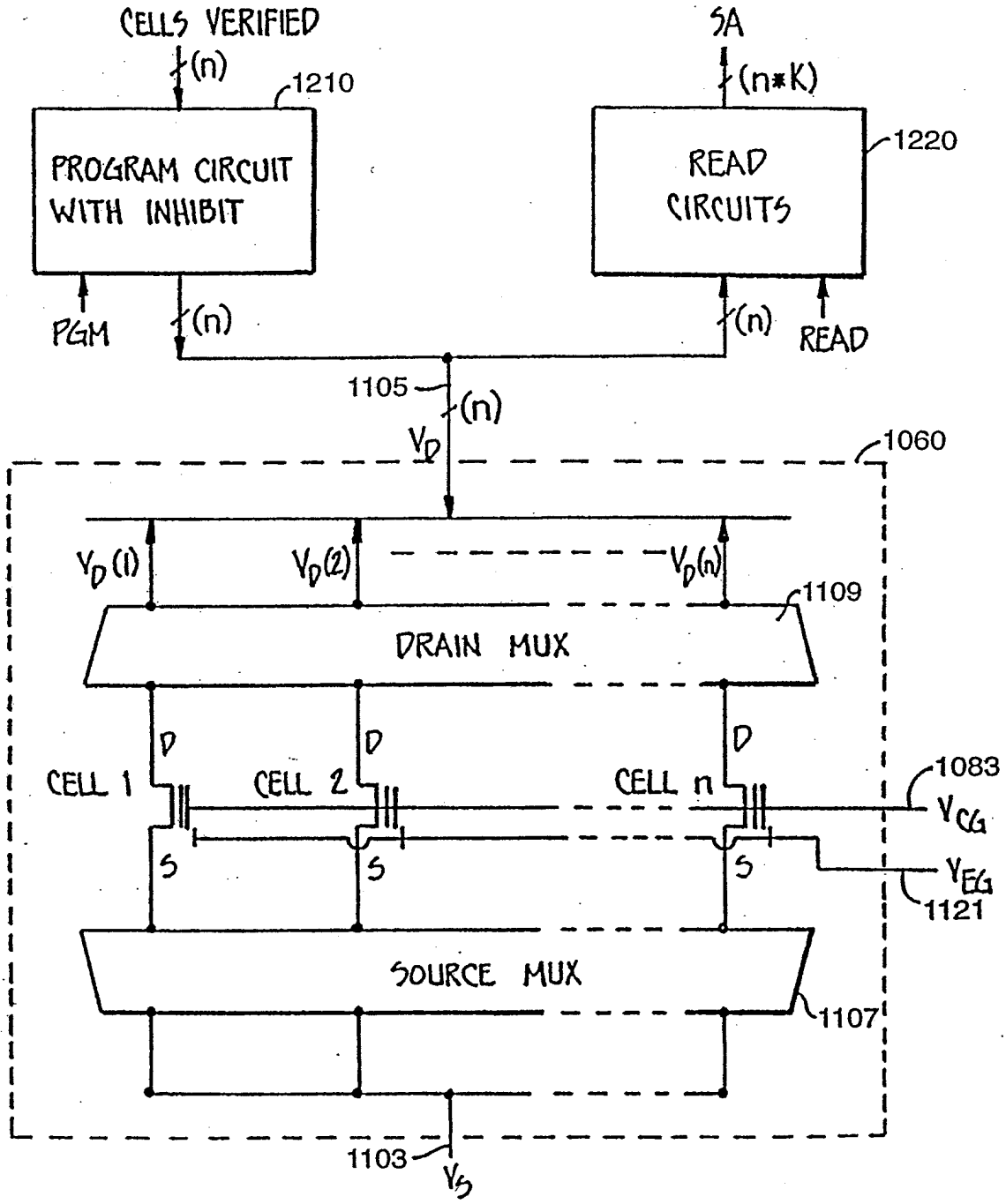


FIG._21C



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG._22